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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/783,598	02/15/2001	Kiyokazu Moriizumi	010153	4350

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EXAMINER
DINH, TUAN T

ART UNIT	PAPER NUMBER
2841	

MAIL DATE	DELIVERY MODE
10/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/783,598	MORIIZUMI, KIYOKAZU	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-16* is/are pending in the application.

4a) Of the above claim(s) *7-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beilin et al. (U.S. Patent 5,916,453) in view of Albrecht et al. (U.S. Patent 4,968,585), and further in view of Ho et al. (U.S. Patent 5,354,712).

As to claim 1, Beilin et al. discloses (see column 6, lines 17-67) a front-and-back electrically conductive substrate as shown in figures 1-17, and in particular figure 9 comprising:

a plurality of posts (18 or 118) extending through the substrate, said post (18) being *anisotropically etched* (because column 6, line 17 states that the post is made by anisotropicall etching (16) to form the post; therefore, the post is anisotropically etched). Each post has an electrically conductive portion (14) that has at least first and second surfaces (figures 7-9 show pads 14 connected on the top and bottom surfaces of the posts 18 for making electrical connection); and an insulative substrate (20).

Beilin et al. does not disclose (16) being *silicon; therefore, does not teach that the form is made by anisotropically etch silicon.*

Albrecht et al. shows micro-miniature tips formed using semiconductor IC technique as shown in figures 1-5 comprising a post (18) being formed by anisotropically etched silicon, see abstract, lines 4-6, column 2, lines 30-37, column 3, lines 9-11, and column 4, lines 16-47).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a layer (16) of Beilin being made of silicon; thereby making post (18 or 118) the post being formed by anisotropically etched silicon, as taught by Albrecht et al. in order to achieve a fine pitch interconnection applied in a high density interconnection of a wiring board or a multilayer substrate by using silicon as a dielectric allowing much more precision than some of the other materials.

Beilin and Albrecht do not specific disclose a side face of the post being covered by an electrically conductive film so as to provide electrical contact between said one side and other side of the substrate.

Ho shows an interconnection structure as shown in figures 1a-1c comprising a side face of an interconnection (31) being covered by an electrically conductive film (22) so as to provide electrical contact between said one side and other side of a substrate (18).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a side face of a post being covered by an electrically conductive film as taught by Ho employed in the substrate of Beilin and Albrecht in order to provide a protection barrier side surfaces for the post.

As to claim 3, Beilin discloses the insulative substrate (20) is composed of an organic resin (column 4, lines 10-35); and the electrically conductive portion (14) is a metal having a melting temperature higher than a melting temperature of an insulation used in the insulative substrate (20), (Note: the melting temperature of metal is higher than the melting temperature of the resin material of the insulative substrate, for example, copper (Cu) having the melting temperature higher than the melting temperature of resin (plastic or silicon et.)).

As to claim 5, Beilin as shown in figure 9 discloses a wiring pattern layer (the wiring is near the pad 14 formed on the top surface) and an insulation layer (another insulative layer 20 on top of the layer 20, see figure 9) is formed on at least the first surface (top surface) of the substrate.

3. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beilin et al. ('685) in view of Albrecht et al. (585), and further in view of Onishi et al. (U.S. Patent 5,459,368).

As to claim 4, Beilin and Albrecht et al. teach the substrate further comprising a pad (14). However, they do not specific disclose pad (14) for mounting a semiconductor component is formed on at least the first surface of the substrate.

Onishi et al. teaches an electronic device (1) as shown in figure 1 mounted on a pad of a substrate.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a pad for mounting a device, as taught by Onishi et al.

employ in the substrate of Beilin and Albrecht et al. for the purpose of providing an excellent electrical connective bonding.

As to claim 6, Beilin and Albrecht et al. do not teach the insulation material of the insulative substrate having compensation of CTE different from the CTE of a mounted semiconductor component. However, Onishi et al. show a surface acoustic wave device mounted module in figure 1 comprising a surface acoustic wave element (1) made of at least one material selected from a group consisting of lithium niobate, lithium tannalate, lithium borate, and quartz, and an insulating resin multiplayer substrate (8), see column 4, lines 36-47. There is a compensation of different material between the multiplayer substrate and the element that would have different CTE therebetween.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the compensation of a different material having different CTE in the substrate of Beilin and Albrecht et al., as taught by Onishi et al., for the purpose of providing the sufficient melting temperature that applied on a component when mounted on a substrate.

Response to Arguments

4. Applicant's arguments filed 08/02/07 have been fully considered but they are not persuasive.

Applicant argues:

a) Beilin and Albrecht in view of Ho, specific of Ho does not disclose or teach "the posts covered by electrical conductive films (specific copper), and also argues about a conformal layer (24) made by TiN, which is less conductive than copper.

Examiner disagrees because first, in claim 1, the applicant is silent recited the conductive film made by copper, and in Ho reference, the conformal layer (24) made by metal, see column 4, lines 37-38, and column 6, lines 10-11 defined that the layer (24) made by metal (TiN) covered the interconnected (31), thus, the combination is meets the claim.

b) Beilin and Albrecht do not teach or suggest "a front and back conductive substrate."

Examiner disagrees as shown in figure 9 of Beilin that shows the front and back conductive substrate because it does contains wiring (14).

c) the combination of Beilin and Albrecht do not the posts 118 must be made by deposition process, i.e. anisotropically etched silicon. Examiner disagrees because the presence of process limitation on product claims, which product does not otherwise patentably distinguish over prior art, cannot impact patentability to the product. In re Stephen 145 USPQ 656 (CCPA 1965), and further for the applicant benefit, Albrecht does disclose shown in figures 1-5 comprising a post (18) being formed by anisotropically etched silicon, see abstract, lines 4-6, column 2, lines 30-37, column 3, lines 9-11, and column 4, lines 16-47).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gutierrez F. Diego can be reached on 571-272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tuan Dnh
October 12, 2007.

TUAN T. DINH
PRIMARY EXAMINER

10/12/07